A Self-Aligning Flip-Chip Assembly Method Using Sacrificial Positive Self-Alignment Structures

Hyung Suk Yang, *Student Member, IEEE*, Chaoqi Zhang, *Member, IEEE*, and Muhannad S. Bakir, *Senior Member, IEEE*

***Abstract*— A self-aligning flip-chip assembly method is described. The method is capable of correcting up to 150 μm (five times the radius of solder balls used) of initial misalignment during flip-chip assembly. Critical components of the self-alignment are four polymeric positive self-alignment structures (PSASs), which are fabricated on a substrate, and four inverted pyramid pits, which are etched on a silicon chip in corresponding positions. The PSAS is removed using solvent after the assembly. Resistance of the solder joints is measured to be below 9 mΩ.**

***Index Terms*— Flip chip, interconnections, microsystems packaging.**

I. Introduction

FLIP CHIP is a high-performance assembly technique that enables area-array interconnections between a chip and a substrate. The technique typically requires an area array of solder balls on a chip or a substrate, and it also requires a flip-chip bonder for aligning and bonding.

In this paper, an enhanced flip-chip technique that can correct a large initial misalignment, up to five times the radius of the solder balls, during the bonding process is presented. The ability to correct a large initial misalignment reduces the accuracy requirement of the flip-chip bonder. In some cases, the assembly may even be performed manually without large, expensive flip-chip bonders, which improves reworkability of the assembled chip and substrate. Thus, the potential benefits of the technique are as follows.

1) Reduction in assembly cost by eliminating the need for flip-chip alignment tools.
2) Increase in assembly throughput by using low-accuracy, high-speed placement tools for applications requiring highly accurate alignment.
3) Ability to perform flip-chip bonding by end-users because the self-alignment capability allows for manual alignment.

The technique uses two novel microfabricated structures to self-align a chip to a substrate: 1) sacrificial positive self-alignment structures (PSASs) and 2) inverted pyramid pits (pits). An overview of the technique is shown in Fig. 1.

Manuscript received January 20, 2015; revised June 15, 2015; accepted July 10, 2015. Date of publication February 17, 2016; date of current version March 10, 2016. Recommended for publication by Associate Editor E. D. Perfecto upon evaluation of reviewers' comments.

The authors are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: jyang@gatech.edu; chqzhang@gatech.edu; muhannad.bakir@mirc.gatech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2015.2467318

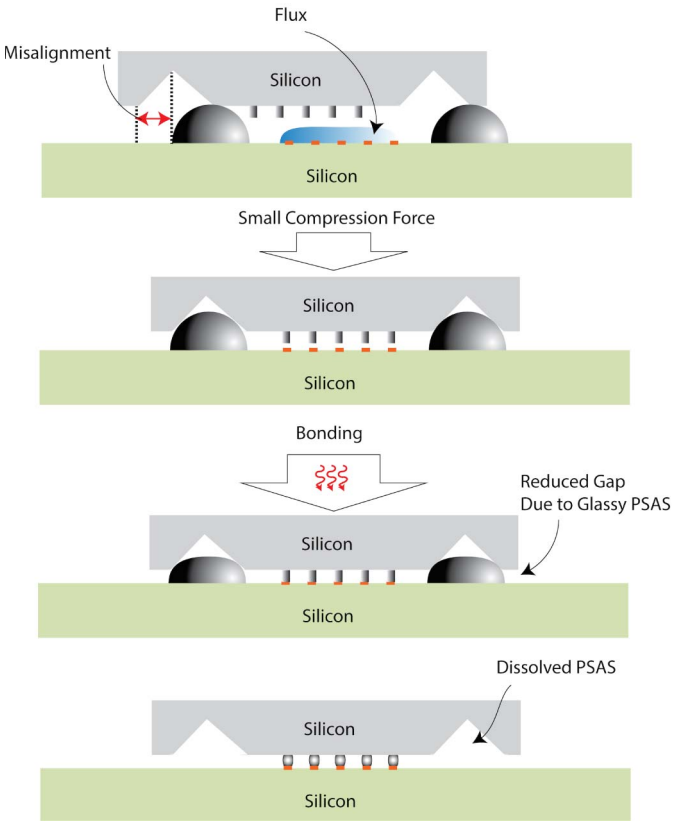

Fig. 1. Brief overview of the tool-less self-alignment bonding process.

II. Background

A. Flip-Chip Bonding

In a conventional flip-chip process involving a chip and a substrate, a flip-chip bonder aligns and brings into contact an area array of pads on the chip to an area array of solder balls on the substrate or vice versa. Next, the chip and the substrate are compressed with a predetermined load and heated with a predetermined reflow profile to form solder joints. Typically, it is also necessary to apply solder flux to solder balls prior to the process.

A survey of commercially available flip-chip bonders and chip placement tools shows that there is an inverse correlation between alignment accuracy and alignment speed. For example, Panasonic's FCB3, a flip bonder with ± 3-μm accuracy, is capable of aligning a chip with a substrate in 1.8 s, while the same company's BM123, a chip placement tool

with ±50-μm accuracy, is capable of aligning a chip with a substrate in 0.12 s [1], [2]. Thus, accurate alignment is costly, and there are significant throughput and cost advantages in being able align to a <5-μm accuracy using a tool with 50-μm accuracy.

The alignment accuracy required depends on the interconnect technology used. For solder-based interconnects, the initial misalignment cannot be greater than the radius of the solder balls because the limited self-alignment capability is provided through molten solder ball's surface tension. For optical-based interconnects, the final misalignment should be <1 μm for optimal coupling performance [3]–[5]; for optical systems with grating couplers, <2-μm misalignment is needed to achieve <1-dB excess loss [4]. Therefore, as interconnect dimensions become smaller and as the industry looks toward optical interconnects, alignment accuracy becomes a critical metric for future systems.

B. Other Self-Alignment Techniques

A number of self-alignment techniques that are compatible with flip-chip assembly have been published previously. For example, surface tensions of flux [6] and water [7] have been used to self-align chips to substrates; however, there are several challenges associated with these techniques. Some examples of the challenges are as follows:

1) Alignment accuracy of the self-alignment techniques that use the entire die surface is limited by the dicing precision, which is limited to ±15 to 25 μm [7].
2) For the self-alignment techniques that exploit pad areas, the magnitude of correctable misalignment is dependent on the pad size. Large pads (i.e., large pitches) are required to correct large initial misalignments.
3) For the self-alignment techniques that exploit water or flux surface tension, the ability to dispense a small volume of water is essential [8]. In addition, leveled surfaces are required [9].

In another study, the sapphire balls and the inverted pyramid pits are used to provide self-alignment [10]; however, the sapphire balls cannot be compressed during the assembly process, which is critical to flip-chip bonding. Another paper presented an alignment using a precisely patterned template and DRIE etched chip edges; however, this approach can be costly, and errors may be introduced while holding the chip in the corner position of the template [11].

The technique presented in this paper can correct large misalignments without being dependent on dimensions and pitches of the interconnect technology used. Moreover, the alignment performance is independent of dicing accuracy and does not require additional tools.

III. Sacrificial Self-Alignment Technology

The PSAS (Fig. 2) and the pits (Fig. 3) are critical components for the presented technique. The PSAS is reflowed photoresist with domelike structures; depending on the initial height of the cylinder-shaped structures that are reflowed, truncated spheres or semispheres may be formed after the reflow. The detailed fabrication process of PSAS and their alignment performance are discussed in [12]. The photoresist material to form PSAS is suitable for this application because the photoresist structure becomes compressible during the thermocompression bonding process, and it can also be easily removed using various types of solvents once the bonding process is complete. Pits are formed using a standard silicon anisotropic etch process using KOH (or alternatively, TMAH).

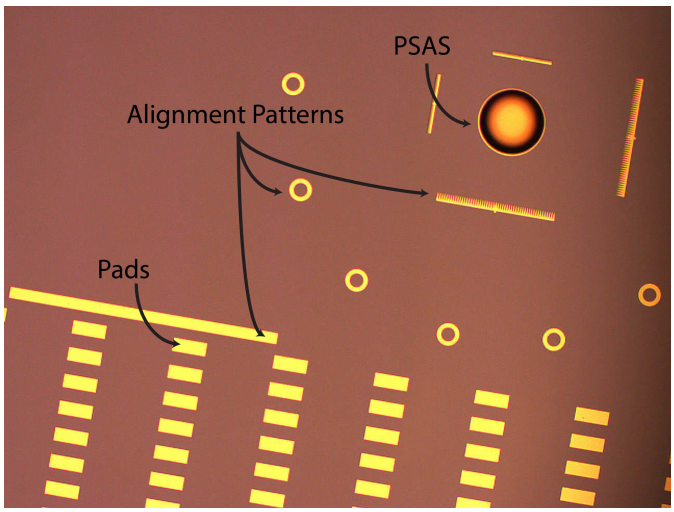

Fig. 2. Microscope image showing a PSAS and pads.

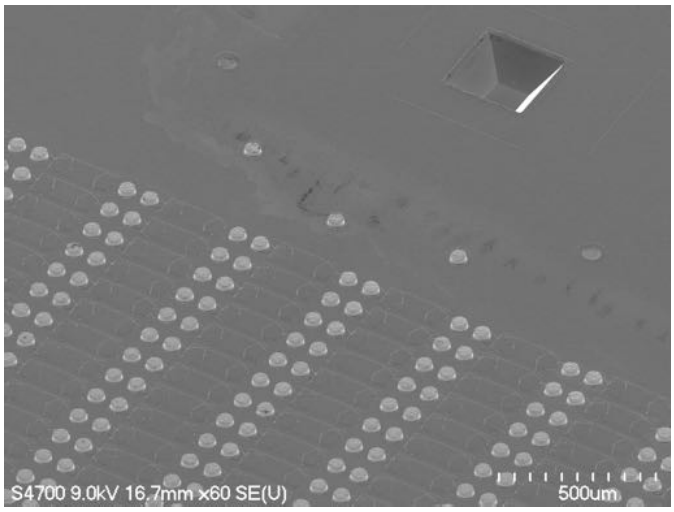

Fig. 3. SEM image showing a pit, solder balls, and traces.

A. Geometrical Considerations

The width of pits and the base diameter of PSAS determine the gap between the chip and the substrate. It is critical that the gap is greater than the height of the solder balls, because premature contact between the solder and the bonding surface could halt the self-alignment process before completion. The equation to calculate the resulting gap has been derived in [13]. In this paper, the pit width and the PSAS base diameter are designed to produce a gap of 28 μm.

The height of the solder balls is 18 μm. Thus, at least 10 μm of vertical compression is required for the solder balls to make contact with the corresponding pads. A smaller gap is desired to prevent the chip from shifting laterally during the

thermocompression process, but a smaller gap also requires that the height of the reflowed solder balls and the accuracy of the gap are controlled more precisely.

The solder balls are formed after the formation of the pits and the metal traces. A silicon dioxide layer (~0.5 μm) is deposited over the metal traces using a PECVD process, and a thick photoresist layer is spin-coated and patterned with circular patterns. Next, circular openings are etched in the silicon dioxide layer using an RIE process. Using the same photoresist layer, 1–2 μm of nickel is electroplated and solder is electroplated subsequently. After removing the photoresist, the solder is reflowed such that the cylinderical solder structures are transformed into the semispherical balls. The photoresist needs to be highly viscous to ensure that the edges of the pits are adequately coated with the photoresist material to prevent electrodeposition of solder or nickel inside or adjacent to the pits.

The width of the pits is also an important parameter because it determines the maximum initial misalignment that can be corrected by the technique. An initial misalignment that is less than half the width of the pits places the center of a PSAS inside the square region of the corresponding pit. As a result, the PSAS is able to slide into the center of the pit when a compressive force is applied. Thus, to enable one to align without a placement tool, it is advantageous to make the initial misalignment tolerance as large as possible. The pits in this paper are fabricated with 300-μm sides, which are large enough for manual assembly.

B. Assembly Process

The flip-chip process flow using sacrificial PSAS is shown in Fig. 4.

1) Placement (Steps 1 and 2): The process assumes that the initial misalignment is less than half the width of the pits. Solder flux is applied to the solder array, and a chip and a substrate are brought into contact. For the purpose of the experiment, a bidirectional camera in a flip-chip bonder is used to intentionally misalign the chip and the substrate [see Fig. 5 (left images)].

2) Inducing Self-Alignment (Step 3): Once the chip and substrate are in contact, a small amount of compressive force is applied to initiate the self-alignment process. As the four PSASs slide into the corresponding pits, the chip and the substrate engage and become locked into place. At this stage, the solder balls are not in contact with the pads because the gap is larger than the height of the solder balls. X-ray imaging is used to verify that the chip and the substrate are correctly aligned [see Fig. 5 (right images)].

3) Thermocompression Bonding (Step 4): Thermocompression bonding is performed using a conventional flip-chip bonding reflow profile. Glassy PSAS become compressible, and the gap between the chip and the substrate is reduced. This allows all solder balls to make contact with the corresponding pads. The compression also compensates for small variations in solder ball height.

4) Flux/PSAS Removal via Water and Acetone Bath With Agitation (Step 5): The bonded sample is submerged in a warm water bath and gently agitated. The water-soluble flux residue is removed during this process. Next, the sample is submerged in an acetone bath and gently agitated. The photoresist-based PSAS is dissolved.

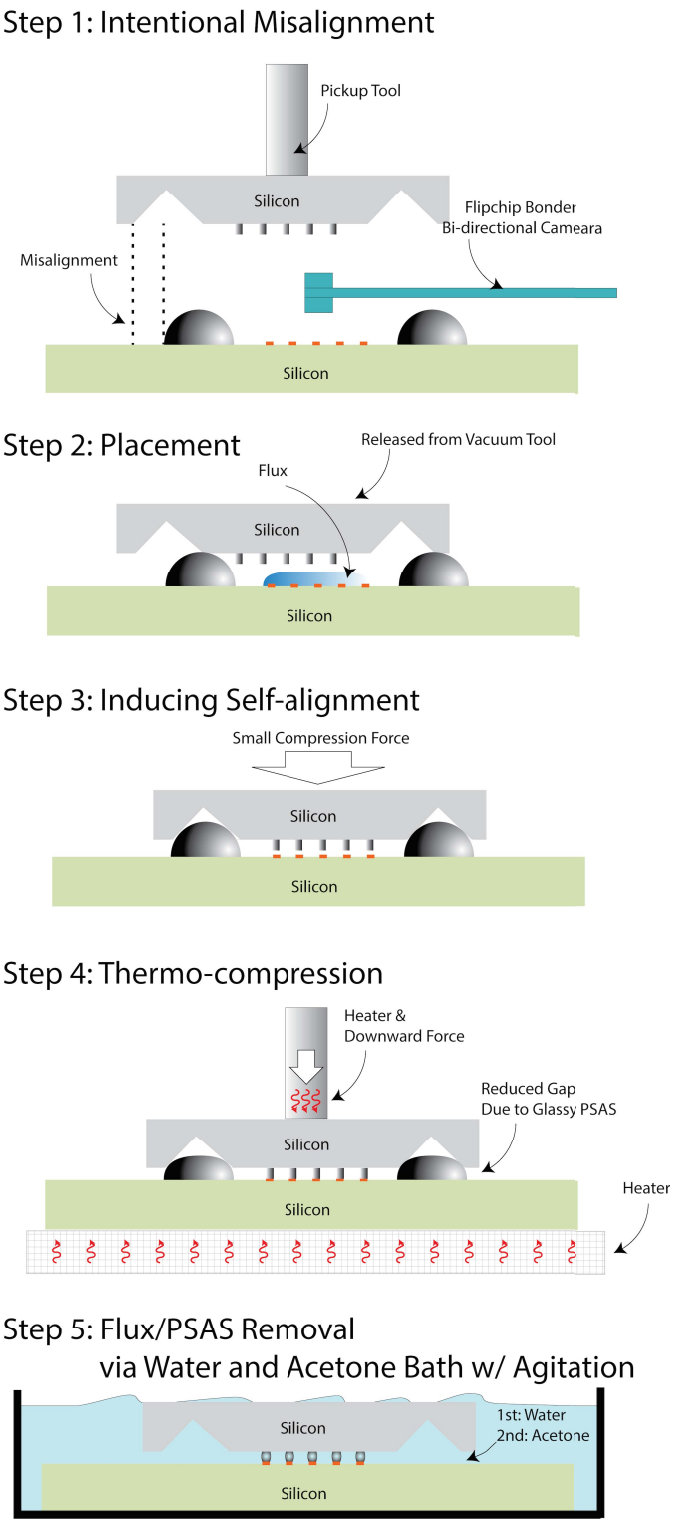

Fig. 4. Experiment to verify the self-alignment capability.

IV. Method and Results

The objective of this paper is to demonstrate that the self-alignment structures can be used sacrificially and that the

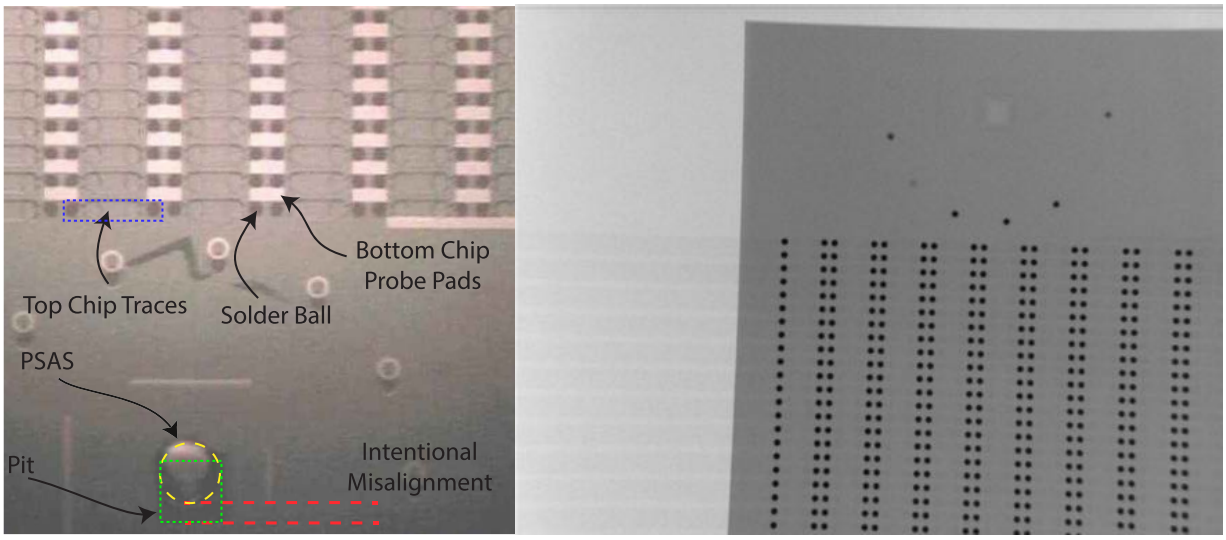

Image showing 60 μm (two times the solder ball radius) of intentional misalignment.

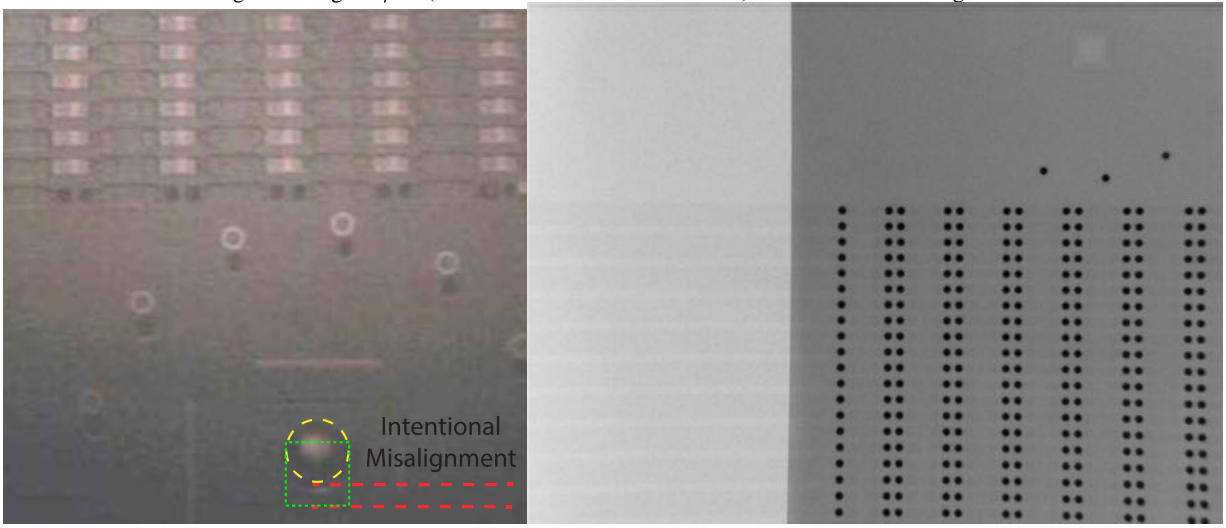

Image showing 120 μm (four times the solder ball radius) of intentional misalignment.

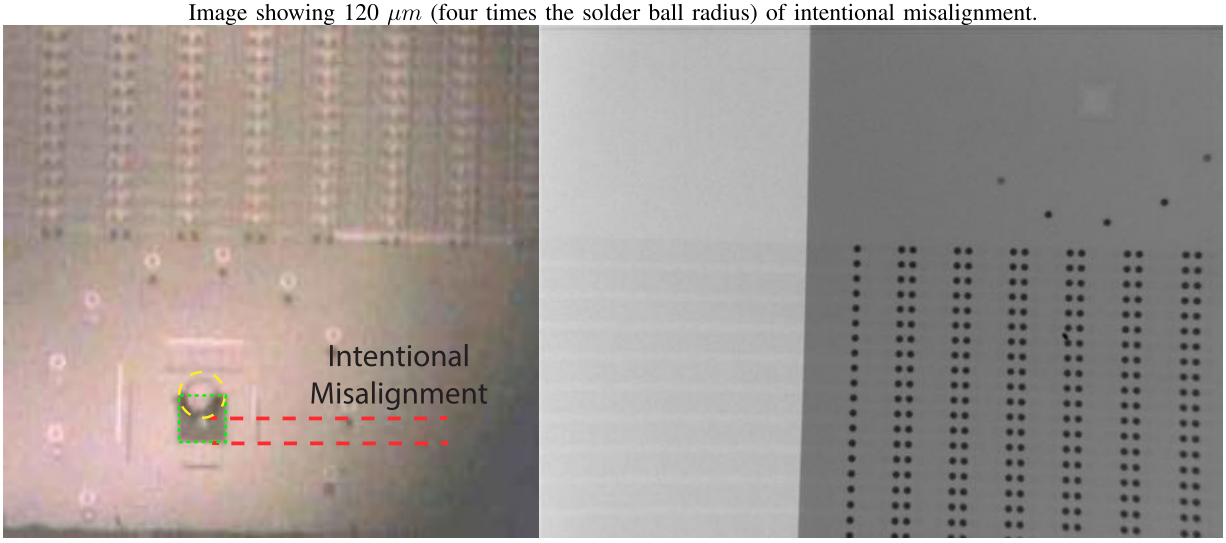

Image showing 150 μm (five times the solder ball radius) of intentional misalignment.

Fig. 5. Images showing the misalignment correction.

technique can be applied in thermocompression bonding of a solder ball array. Experiment details are outlined in Table I. The technique is demonstrated in three parts.

1) The ability to correct misalignment beyond what is possible with conventional flip-chip processes is verified. A lateral misalignment as large as 150 μm, which is

TABLE I
EXPERIMENT DETAILS

Chip Parameters	
Top Chip Dimensions	1.8 cm x 1.6 cm
Bottom Chip Dimensions	2.7 cm x 2.7 cm
Chip Thicknesses	500 μm
Silicon Wafer Type	<100> n-type doped
Solder Parameters	
Solder Type	$Sn_{60}Pb_{40}$
Solder Deposition Method	Electroplating
Solder Diameter	60 μm
Solder Height (Pre-reflow)	18 μm
Array Size (row x col = total)	130 x 84 = 10920
Pad Parameters	
Top Chip UBM	
(Below Solder)	1-2 μm of Ni
	1 μm of Cu
(Above Si Nitride)	50 nm of Ti
Bottom Chip Pad Materials	
(Top Exposed Layer)	30 nm of Au
	1-2 μm of Ni
	1 μm of Cu
(Above Si Nitride)	50 nm of Ti
Assembly Parameters	
Pre-bonding Gap	28 μm
Bonding Force	4 N
Flux	Indium Corporation FC-NC-HT-A1

five times the radius of the solder balls, is intentionally induced during the initial chip placement. After applying a small compression force to induce self-alignment, the final relative position of the chip and substrate is determined using an X-ray imaging tool [Fig. 4 (Steps 1–3)].

2) Compressibility of the PSAS during the thermocompression bonding process is verified. The electrical connectivity between the chip and the substrate is verified using a set of daisy chain structures that are designed into the mask design [Fig. 4 (Step 4)].
3) The ability to use the PSAS sacrificially is verified. The assembled sample is submerged in a resist remover solution to ensure that PSAS can be removed after the assembly process. The assembled samples are separated and examined with an SEM and optical microscope [Fig. 4 (Step 5)].

A. Misalignment Correction

The objective of this section is to verify that the PSAS and the pits can correct initial misalignments larger than the self-alignment capabilities of a solder ball array. Typically, the solder ball arrays can correct misalignments that are equal to or less than the radius of the largest solder balls used during the bonding process, and a highly accurate alignment

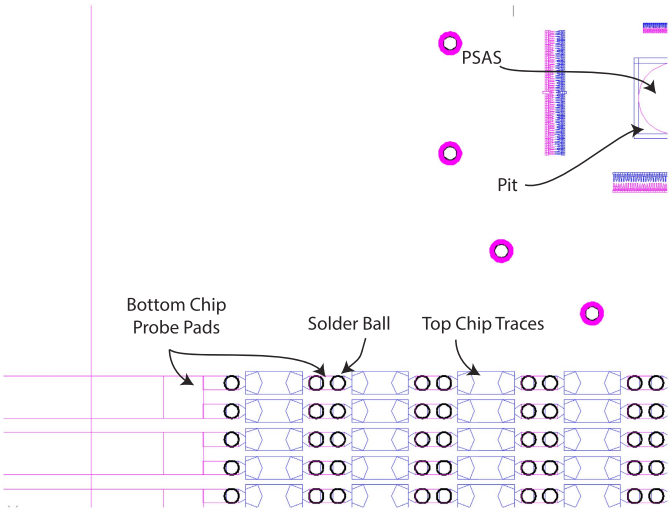

Fig. 6. Mask design of the chip and the substrate that are perfectly aligned to each other.

accuracy can be achieved if the process is optimized [14]. However, it is often desirable to have smaller solder balls with small pitches while attaining the alignment capability of larger solder balls. For example, an application may require a dense array of solders with 30-μm diameters as well as a self-alignment capability that can correct up to 150 μm of misalignment. Using the conventional process, only up to 15 μm of misalignment can be corrected in such case, and a misalignment >15 μm may result in solder balls becoming assembled with wrong pads.

Using the PSAS and pits, it is possible to decouple these two requirements. To demonstrate this, three samples are aligned with an intentional misalignment of 60 μm ($2 \times r_{\text{solder}}$), 120 μm ($4 \times r_{\text{solder}}$), and 150 μm ($5 \times r_{\text{solder}}$). The r_{solder} represents the radius of the solder balls, which is 30 μm. The intentional misalignment is induced using a flip-chip bonder, and the images captured using the bonder's bidirectional camera before chip placement are shown in Fig. 5. For easy comparison, Fig. 6 shows the mask design with the perfect alignment, and Fig. 7 shows the perfectly aligned image captured by the bidirectional camera.

Each chip is released from the vacuum tool after being placed on top of a pad array with the intentional misalignment. Next, a small weight is applied to the chip until the chip and the substrate lock into place. At this point, the chip cannot be moved laterally. Fig. 5 shows the images captured before and after the alignment process with various initial misalignments that are intentionally introduced. In all three cases, the X-ray images show that the solder balls are correctly aligned to the intended pads despite large misalignments. Fig. 8 shows the bonded chip on the substrate.

B. Thermocompression Assembly and Electrical Connectivity

The objective of this section is to verify that the PSAS and the pits are compatible with the thermocompression bonding process; the bonding quality (i.e., resistance) of the solder balls and the yield are measured. Using the three samples

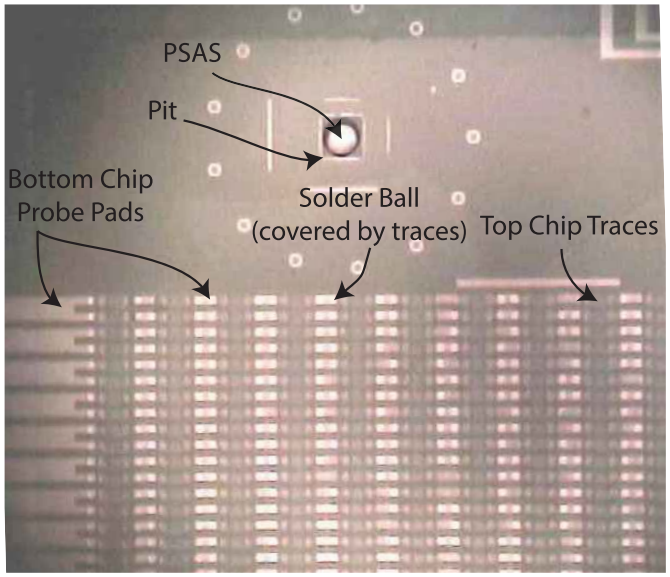

Fig. 7. Overlay captured by the flip-chip bonder's bidirectional camera shows a chip and a substrate that are perfectly aligned.

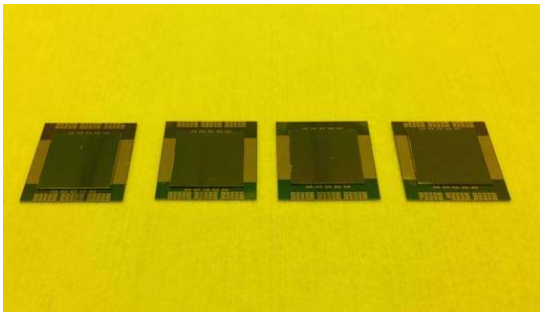

Fig. 8. Image showing four pairs of bonded samples.

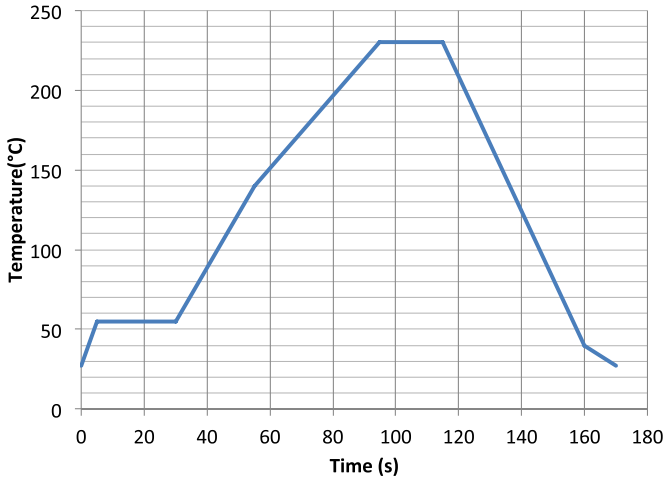

Fig. 9. Reflow profile used for the assembly process.

from the first set of experiments, thermocompression bonding is performed. A constant compressive force (4 N) was used, and the reflow temperature profile used is shown in Fig. 9.

Two types of electrical structures are built-in to the chips and substrates:

TABLE II
RESISTANCE MEASUREMENTS

Sample No.	Init. Misalignment	Location No.	Total R ($m\Omega$)	Total R - $R_{pad/wire}$ ($m\Omega$)
1	60 μm	1	17	7.67
		2	20	10.67
		3	19	9.67
		4	17	7.67
		Avg.	18.25	**8.92**
2	120 μm	1	17	7.67
		2	18	8.67
		3	19	9.67
		4	17	7.67
		Avg.	17.75	**8.42**
3	150 μm	1	19	9.67
		2	18	8.67
		3	17	7.67
		4	17	7.67
		Avg.	17.25	**8.42**

1) Daisy chain structures are used to verify that the bonding process provides high yield. Daisy chain sizes ranging from 84 solder balls to 10 920 solder balls are included in the layout.
2) Resistance of a single solder ball is measured to verify that the high-quality bonds have been formed.

The electrical measurements are shown in Table II. The results show that the high quality solder bonds are formed, and that the yields calculated from the daisy chain measurements are 100%. Subsequent detaching of the chip and the substrate shows that 100% of the solder balls (including the pads underneath) are transferred from the top chip to the bottom chip, which indicates that the newly formed bonds are stronger than the adhesion strength of the evaporated titanium and copper on a silicon nitride surface.

C. PSAS Removal

The objective of this section is to verify that the PSAS can be removed after a thermocompression assembly. Since the PSAS is made of photoresist, the structures' presence beyond the assembly process can cause reliability issues, and they must be removed. However, while photoresists can typically be removed easily, there are two factors that may affect the ability to remove PSAS: 1) the temperature of the bonding process and 2) the gap between the chip and the substrate. As such, the removal process warrants verification.

Flux is removed prior to the removal of the PSAS. Solder flux from the Indium Corporation is used and can be removed by a warm water bath with a gentle agitation. To remove the PSAS, the bonded samples are submerged in resist remover solvent. Fig. 10 shows the images of detached chips that underwent the PSAS removal process. The images show that the PSAS is completely removed.

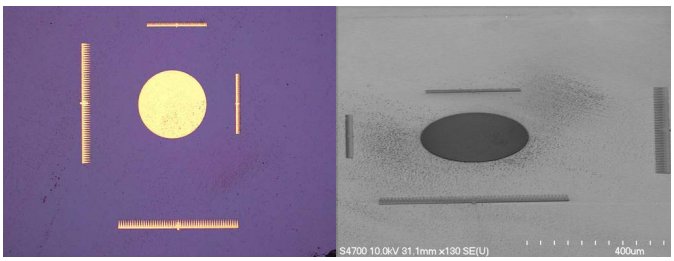

Fig. 10. SEM and microscope images of detached chips show that the PSAS is completely removed.

V. Conclusion

A thermocompression bonding of a solder ball array is demonstrated using sacrificial PSAS and inverted pyramid pits. By intentionally introducing a lateral misalignment greater than what can be corrected with the surface tension of solder balls, the ability to correct up to 150 μm of misalignment using the PSAS and pits is experimentally verified. In addition, high-quality bonding is also verified through electrical measurements, and the ability to remove the PSAS after the bonding process is visually verified.

Acknowledgment

The authors would like to thank Dr. H. Thacker and Dr. J. Mitchell at Oracle Labs for valuable feedbacks, guidance, and support, and AZ Electronic Materials and Capitol Scientific Inc. for providing the AZ 40XT-11D photoresist used to fabricate the positive self-alignment structures in this paper. They would also like to thank R. Eakin for troubleshooting problems related to photolithography.

References

[1] Panasonic Corporation of North America. (2012). *Panasonic BM123-133 Flyer*. [Online]. Available: http://www.panasonicfa.com/pdfs/BM123-133.pdf

[2] Panasonic Corporation of North America. (2012). *Panasonic FCB3 Flyer*. [Online]. Available: http://www.panasonicfa.com/pdfs/FCB3.pdf

[3] X. Zheng *et al.*, "Ultralow power 80 Gb/s arrayed CMOS silicon photonic transceivers for WDM optical links," *J. Lightw. Technol.*, vol. 30, no. 4, pp. 641–650, Feb. 15, 2012.

[4] J. Yao *et al.*, "Grating-coupler based low-loss optical interlayer coupling," in *Proc. 8th IEEE Int. Conf. Group IV Photon. (GFP)*, Sep. 2011, pp. 383–385.

[5] A. Majumdar, J. E. Cunningham, and A. V. Krishnamoorthy, "Alignment and performance considerations for capacitive, inductive, and optical proximity communication," *IEEE Trans. Adv. Packag.*, vol. 33, no. 3, pp. 690–701, Aug. 2010.

[6] Y. Ito, T. Fukushima, K.-W. Lee, K. Choki, T. Tanaka, and M. Koyanagi, "Flux-assisted self-assembly with microbump bonding for 3D heterogeneous integration," in *Proc. IEEE 63rd Electron. Compon. Technol. Conf. (ECTC)*, May 2013, pp. 891–896.

[7] F. Sun, Y. Leblebici, and T. Brunschwiler, "Surface-tension-driven multi-chip self-alignment techniques for heterogeneous 3D integration," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 1153–1159.

[8] K.-W. Lee, S. Kanno, K. Kiyoyama, T. Fukushima, T. Tanaka, and M. Koyanagi, "A cavity chip interconnection technology for thick MEMS chip integration in MEMS-LSI multichip module," *J. Microelectromech. Syst.*, vol. 19, no. 6, pp. 1284–1291, Dec. 2010.

[9] T. Fukushima *et al.*, "Surface tension-driven chip self-assembly with load-free hydrogen fluoride-assisted direct bonding at room temperature for three-dimensional integrated circuits," *Appl. Phys. Lett.*, vol. 96, no. 15, p. 154105, 2010. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/96/15/10.1063/1.3328098

[10] I. Shubin *et al.*, "A novel MCM package enabling proximity communication I-O," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 224–229.

[11] Q. Chen *et al.*, "A novel chip-to-wafer (C2W) three-dimensional (3D) integration approach using a template for precise alignment," *Microelectron. Eng.*, vol. 92, pp. 15–18, Apr. 2012. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931711004710

[12] H. S. Yang, C. Zhang, and M. S. Bakir, "Self-aligned silicon interposer tiles and silicon bridges using positive self-alignment structures and rematable mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 11, pp. 1760–1768, Nov. 2014.

[13] H. S. Yang, C. Zhang, and M. S. Bakir, "Self-alignment structures for heterogeneous 3D integration," in *Proc. IEEE 63rd Electron. Compon. Technol. Conf. (ECTC)*, May 2013, pp. 232–239.

[14] H. D. Thacker *et al.*, "Flip-chip integrated silicon photonic bridge chips for sub-picojoule per bit optical links," in *Proc. 60th Electron. Compon. Technol. Conf. (ECTC)*, Jun. 2010, pp. 240–246.

Hyung Suk Yang received the B.S. (Hons.) degree in computer engineering, the M.S. degree in electrical and computer engineering, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2007, 2008, and 2014, respectively.

He has authored or co-authored 15 journal publications and conference proceedings. His current research interests include 3-D heterogeneous integration using novel microfabricated interconnect technologies.

Mr. Yang was a co-recipient of the 2009 and 2010 SRC TECHCON Best in Session Paper Award, the 2009 IMAPS Best Student Paper Award, and the 2009 IMAPS Best in Session Paper Award. He was a recipient of the Intel Corporation Ph.D. Fellowship from 2011 to 2012.

Chaoqi Zhang received the B.S. degree in physics from Shandong University, Jinan, China, in 2005, the M.S. degree in microelectronics from Tsinghua University, Beijing, China, in 2008, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2015.

He is currently a Senior Hardware Engineer with the Netra Systems and Networking Group, Oracle, San Diego, CA, USA, where he is involved in advanced packaging technologies and platforms for electric and silicon photonic systems.

Muhannad S. Bakir received the B.E.E. degree from Auburn University, Auburn, AL, USA, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 2000 and 2003, respectively.

He is currently an Associate Professor and the ON Semiconductor Junior Professor with the School of Electrical and Computer Engineering, Georgia Tech. His areas of interest include 3-D electronic system integration, advanced cooling and power delivery for 3-D systems, biosensors and their integration with CMOS circuitry, and nanofabrication technology.

Dr. Bakir is the recipient of the 2013 Intel Early Career Faculty Honor Award, the 2012 DARPA Young Faculty Award, the 2011 IEEE CPMT Society Outstanding Young Engineer Award, and was an Invited Participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium. In 2015, he was elected by the IEEE CPMT Society to serve as a Distinguished Lecturer for a four-year term. He and his research group have received 14 conference and student paper awards including five from the IEEE Electronic Components and Technology Conference, four from the IEEE International Interconnect Technology Conference, and one from the IEEE Custom Integrated Circuits Conference. His group was awarded the 2014 Best Paper of the IEEE Transactions on Components Packaging and Manufacturing Technology in the area of advanced packaging. He is an Editor of the IEEE Transactions on Electron Devices and an Associate Editor of the IEEE Transactions on Components, Packaging and Manufacturing Technology.